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21171 7590 01/08/2007

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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/807,286	03/24/2004	Tetsuo Kawano	1450.1040	3924

TITLE OF INVENTION: SEMICONDUCTOR INTEGRATED CIRCUIT TIMING ANALYSIS **APPARATUS** TIMING ANALYSIS METHOD AND TIMING ANALYSIS PROGRAM

-- APPARATUS, --

APPLN. TYPE	SMALL ENTITY	ISSUE FEE DUE	PUBLICATION FEE DUE	PREV. PAID ISSUE FEE	TOTAL FEE(S) DUE	DATE DUE
nonprovisional	NO	\$1400	\$300	\$0	\$1700	04/09/2007

EXAMINER	ART UNIT	CLASS-SUBCLASS
GARBOWSKI, LEIGH M	2825	716-006000

1. Change of correspondence address or indication of "Fee Address" (37 CFR 1.363).	2. For printing on the patent front page, list (1) the names of up to 3 registered patent attorneys or agents OR, alternatively, (2) the name of a single firm (having as a member a registered attorney or agent) and the names of up to 2 registered patent attorneys or agents. If no name is listed, no name will be printed.	1 STAAS & HALSEY LLP
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(A) NAME OF ASSIGNEE

FUJITSU LIMITED

(B) RESIDENCE: (CITY and STATE OR COUNTRY)

KAWASAKI, JAPAN

Please check the appropriate assignee category or categories (will not be printed on the patent): Individual Corporation or other private group entity Government

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Date

April 6, 2007

Typed or printed name

H. J. STAAS

Registration No.

22,010

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